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METHOD AND APPARATUS FOR PRODUCING A CLOCK OUTPUT SIGNAL

Background of the Invention:

Field of the Invention:

The present invention relates to a method and apparatus for producing a clock output signal, and in particular, but not exclusively, to a delay circuit for a clock having an infinitely adjustable delay for use in delay locked loop (DLL) circuits. The invention also relates to a charge pump and to a control loop of a delay locked loop.

DLL circuits are known, among other things, from U.S. Patent No. 5,015,872 and also from the publication by Thomas H. Lee et al. in IEEE Journal of Solid State Circuits, Vol. 29, No. 12, December 1994. The drawback in these circuits is that the clock input frequency is halved before phase shifting, in order to be doubled subsequently, i.e. after phase shifting. This can be problematic at high clock frequencies, or may require very fast and precise EXOR gates and mixers. Nonlinearities may also arise in this context.

In addition, when window comparators are produced which monitor the control voltage and control the actual delay generator, as in the aforementioned publication by Lee et al.

("quadrant boundary detector"), problems arise in the changeover, as shown in Fig. 1. Fig. 1 shows a comparison between an ideal curve and a real curve. Apart from the nonlinearity of the twisting (real) curve, which changes the loop gain of the DLL loop, a phase jump generally occurs at the changeover point (e.g. at 180°), because the changeover point cannot be set with absolute certainty (tolerances). This means that particular phase adjustments cannot be made and oscillation may occur (abrupt switching between the phases $180°-\Delta\varphi°$ and $180°+\Delta\varphi°$ when the desired phase is situated in between).

Summary of the Invention:

It is accordingly an object of the invention to provide an apparatus for producing a clock signal, a control loop, a charge pump, and a method for producing a clock signal which overcome the above-mentioned disadvantages of the prior art apparatus and methods of this general type.

With the foregoing and other objects in view there is provided, in accordance with the invention, a method for producing a clock output signal, that includes steps of: receiving an input signal that contains an information item representing a phase; producing a plurality of clock signals having phases that are respectively shifted from one another by a predetermined amount; weighting each one of the plurality

of the clock signals in dependence on the information item that is contained in the input signal; and mixing the weighted clock signals in order to produce a clock output signal having a phase that essentially matches the phase that is represented by the phase information item.

With this method, it is thus possible to dispense with halving the clock frequency. Instead, the original clock frequency is retained and suitable phase shifts are used to produce a clock output signal, which has the desired phase.

In particular, the method preferably involves producing a clock input signal of a predetermined frequency, which signal is duplicated by repeated phase shifting, so that the aforementioned multiplicity of clock signals are obtained which all have the predetermined frequency. This "clock signal multiplication" with the retention of a clock input signal frequency can be used to produce a desired phase, as mentioned, by means of subsequent weighting and mixing, without the need to perform any disadvantageous frequency halving on the clock signal.

In accordance with an additional mode of the invention, the multiplicity of clock signals are four clock signals whose phases are shifted from one another by 90° and which are

preferably produced from the clock input signal by using a quadrature oscillator.

In accordance with an additional mode of the invention, the weighted clock signals are mixed by addition. Furthermore, it is possible to carry out band-limiting in order to filter out harmonics when mixing the weighted clock signals.

With the foregoing and other objects in view there is provided, in accordance with the invention, an apparatus for producing a clock output signal, that includes: an input for receiving an input signal containing a phase information item representing a phase; a clock generator for producing a plurality of clock signals having phases that are shifted from one another by a predetermined amount; and a weighting and mixing circuit for weighting each one of the plurality of the clock signals based on the phase information item to obtain a plurality of weighted clock signals. The weighting and mixing circuit is also for mixing the plurality of the weighted clock signals to produce a clock output signal having a phase that essentially matches the phase represented by the phase information item.

This apparatus may, by way of example, be part of a delay lock loop control loop. The clock generator can be formed by a

quadrature oscillator for producing four clock signals whose phases are shifted from one another by 90°.

With the foregoing and other objects in view there is provided, in accordance with the invention, a control loop, that includes: a phase shifter for producing a first clock phase; a phase detector for detecting a phase difference between a second clock phase and the first clock phase, the phase detector producing an output signal based on the detected phase difference; a charge pump for integrating the output signal of the phase detector, the charge pump having an integration polarity; and a controller for changing over the integration polarity of the charge pump at predetermined switching points based on the detected phase difference. The switching points are subject to hysteresis. This apparatus eliminates the drawbacks mentioned in the introduction of adjustment points, which can be adjusted only imprecisely and also of undesirable oscillation. In particular, the "phase hole" φ° shown in Fig. 1 is avoided.

In accordance with an added feature of the invention, such a control loop can be used in delay lock loop circuits.

With the foregoing and other objects in view there is provided, in accordance with the invention, a method for producing a clock signal, that includes: detecting a phase

difference between a clock phase of a first input signal for a phase shifter and a clock phase of a first output signal of the phase shifter; producing a second output signal based on the detected phase difference; producing a second input signal for the phase shifter by integrating the second output signal; and changing over a polarity of the integrating at predetermined switching points based on the detected phase difference, the switching points being subject to hysteresis.

With the foregoing and other objects in view there is provided, in accordance with the invention, a charge pump for producing an output signal that includes a charge pump circuit for receiving an input signal having a phase. The charge pump circuit is also for producing an output signal having a phase. The output signal is either a proportional signal essentially proportional to the phase of the input signal or an inversely proportional signal essentially inversely proportional to the phase of the input signal. The charge pump circuit is designed such that the output signal changes between the proportional signal and the inversely proportional signal at predetermined switching points at which a predetermined jump in the phase of the output signal takes place.

In accordance with an additional feature of the invention, the switching points are preferably subject to hysteresis.

In accordance with a concomitant feature of the invention, the predetermined jump is advantageously a phase return of predetermined magnitude.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in method and apparatus for producing a clock output signal, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

<u>Brief Description of the Drawings</u>:

Fig. 1 shows a voltage characteristic when the polarity of a charge pump changes over in a known DLL circuit;

Fig. 2 schematically shows a block diagram of a DLL circuit having a phase shifter based an exemplary embodiment of the invention;

Fig. 3 shows a circuit, contained in the phase shifter from Fig. 2, for producing a clock output signal;

Fig. 4 shows a control circuit, which is likewise contained in the phase shifter from Fig. 2, for selecting and controlling input clocks for the circuit from Fig. 3;

Fig. 5 shows the four clock input signals for the circuit from Fig. 3;

Fig. 6 shows the signals for the control circuit from Fig. 4 (where In is proportional to Un);

Fig. 7 shows control current and phase waveforms for a circuit in accordance with a further refinement of the invention;

Fig. 8 shows the changeover of the polarity of a charge pump with hysteresis;

Fig. 9 shows a circuit employing the waveforms shown in Figs. 7 and 8; and

Fig. 10 is a table summarizing the properties of the control circuit shown in Fig. 4 (signals S0 to S3, U0 to U3) as a function of the input U_{CP} (output of the charge pump).

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 2 thereof, there is shown an illustrative delay locked loop (DLL) circuit 1 containing a phase shifter 2 in accordance with a refinement of the invention. The DLL circuit 1 also has a phase detector 3 and a charge pump 4. The phase detector 3 has an input I for receiving a data signal. The data signal is additionally supplied to an input I of the logic unit 5, which is clocked by a clock output signal Cout of the DLL circuit 1 via a clock input T. The purpose of the DLL circuit 1 is to provide a clock signal Cout, which is in phase with the pulse timing of the data signal. DLL circuits as such are known and are therefore not explained in more detail here.

Figs. 3 and 4 show the circuit contained in the phase shifter 2 from Fig. 1. Fig. 3 shows a circuit for producing the clock signal C_{out} by mixing the clock signals C0 to C3. These four clock signals C0 to C3 are shown in Fig. 5. The circuit contains two mixers, which are respectively operated with the appropriate clock phases and operate differentially on the same load resistors R1 and R2. A capacitor C1 (optional) is

used for band-limiting, since only the fundamentals of the individual phases of the clock signals C1 to C3 need to be mixed (added), and harmonics need to be filtered out accordingly. The control voltages U0 to U4 are used to weight the respective clock signals C0 to C3 in an appropriate manner.

The circuit shown does not use the halved clock frequency (as in the prior art), but rather uses the original clock frequency, which contains the appropriate phase shift as a result of suitable phase shifter circuits. This means that a total of four clock phases are admittedly necessary; since, however, in each case two of these clock signals are inverted with respect to one another, they are easily available anyway (Cxq is the inverted clock signal of Cx, C0 = C2q, C0q = C2, C1 = C3q, C3 = C1q in Figs. 3, 5 and 9). These phases can, by way of example, be produced using a quadrature oscillator which produces the clock signals denoted in Fig. 5 by 0° and 90° and also the respectively inverted clock signals 180° and 270°.

The clock signals are selected and controlled by the control circuit shown in Fig. 4 in order to produce the control voltages U0 to U3. Fig. 6 shows the control signals produced by the circuit shown in Fig. 4 for the purpose of mixing the clock signals (where the currents I0 to I3 are proportional to

the voltages U0 to U3). The switching elements RS0 to RS3 in Fig. 4 are RS flip-flop circuits (reset-set), and K0 to K3 are comparators. The comparators K0 to K3 are adjusted such that they trigger a changeover operation as soon as the control voltages U0 to U3 reach the upper or lower limitation, i.e. no further phase shift can be achieved. The changeover operation is triggered by triggers from the flip-flop circuits. Changeover takes place such that the signals shown in Fig. 6 are generated.

As already indicated above, one advantage of this circuit is the use of the original clock frequency, and not of half the clock frequency, as in the aforementioned known circuits. This eliminates the problematical frequency doubling which is required in these circuits.

Fig. 6 likewise shows the control signals S0 to S3 for controlling the mixer and the amplifier SDiff (single-ended push-pull converter). Since only one of the mixers is controlled in each case, the respective inactive amplifier needs to be turned off or switched to a fixed potential, under the control of the signals S0 to S3. In addition, in accordance with the requirements, the gain of the amplifier SDiff also needs to be either 1 or -1, likewise under the control of the signals S0 to S3. Fig. 10 is a table

summarizing the properties of the amplifier SDiff as a function of the control inputs S0 to S3.

Another refinement of the invention provides a circuit, which avoids the aforementioned problem of the "phase holes" as a result of appropriate overlapping of the resulting phase positions. For this purpose, a return in phase takes place at the changeover points of the polarity of the charge pump 4 (Fig. 2), as shown in Figs. 7 and 8. This admittedly results in a phase jump during the synchronization phase. In the steady state, however, no further return can take place if there is appropriate hysteresis. (Only in the case of relatively large phase modulation in a frequency range, which is narrower than the bandwidth of the DLL circuit 1 could a phase jump nevertheless occur. This is improbable in the real application, however. In addition, the phase jump can be kept so small that no bit errors arise).

Fig. 9 shows one implementation of the circuit of this refinement. Connected in parallel with the differential stages T10 to T13 are further differential stages T10a to T13a and T10b to T13b, which increase the size of the phase amplification $\Delta\varphi/dUx$ (Ux is the respective differential control voltage U0-U2, or U1-U3). The increase in the size of the phase amplification depends on the dimensioning of T14x, T15x or the currents thereof, and also on R7x to R10x. Since

the currents in the mixer are connected and disconnected by S0 to S3 (using the switches S0 to S7 in Fig. 9, under the control of the signals of the same name from Fig. 4), the phase profile shown at the bottom of Fig. 7 with the described overlaps (or phase jumps) at 45°, 135°, 225° and 315° is produced. Mathematically, this can be described for the quadrants $45° < \varphi < 135°$ as follows:

$$C_{out} = C0 * I_{T10}(U0) + C2 * I_{T11}(U2) + C1 * I_{T12}(max) + C3 * I_{T13a}(U2),$$

where $I_{T10} = 1...0$, $I_{T11} = 0...1$, $I_{T13a} = 0.1 * I_{T13}$.

If it is assumed that $Cx = \sin(\omega t + 90° * x)$, $x = 0, 1, 2, 3$, a resulting phase is produced which corresponds to the mean value of the three phases plus the small component of the fourth phase, i.e. the respective component of the currents controls the phase angle. The clock signal C1 is supplied permanently (using factor 1). The clock signal C0 is reduced to the same extent as the clock signal C2 is input at increased level. In addition, a small component of C3 is input so that a phase of more than 90° (e.g. 100°) can be covered in a quadrant. By adding this small component of the respective fourth current (in this case I_{T13a}), the phase amplification is increased and the overlap is attained. This component determines the phase overlap.

The current values used in the formula are normalized, i.e. $I_{T11max} = 1$, $I_{T11min} = 0$, for example.

The invention is not limited to the exemplary embodiments described, but instead comprises modifications within the context of the scope of protection defined by the claims.